

## Interfacing Signalscan waveform viewer

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Signalscan is a waveform viewer used to analyze and trouble-shoot simulation results from VHDL/Verilog.

1. Synthesize the VHDL code in the ac\_shell using the following command and quit.

```
> source name.tcl
```

ALU design (project1) example:

```
> source alu32.tcl
```

2. Open the test bench (eg alu32\_tb.v) and type the following before **endmodule**

```
initial begin
$shm_open("name.shm");
$shm_probe(pin1,pin2,...etc);
end
```

example:

```
initial begin
$shm_open("alu32.shm");
$shm_probe(a,b,d,Cin,Cout,V,S);
end
```

Save and close.

3. Simulate the design using the following command on the console:

```
verilog test_bench_name verilog_netlist_name -v library path
```

example:

```
verilog alu32_tb.v alu32.v -v /x/lgjohn/public/lib/ami350hxsc.d.lib
```

4. On the console type **signalscan&** which opens the waveform window.

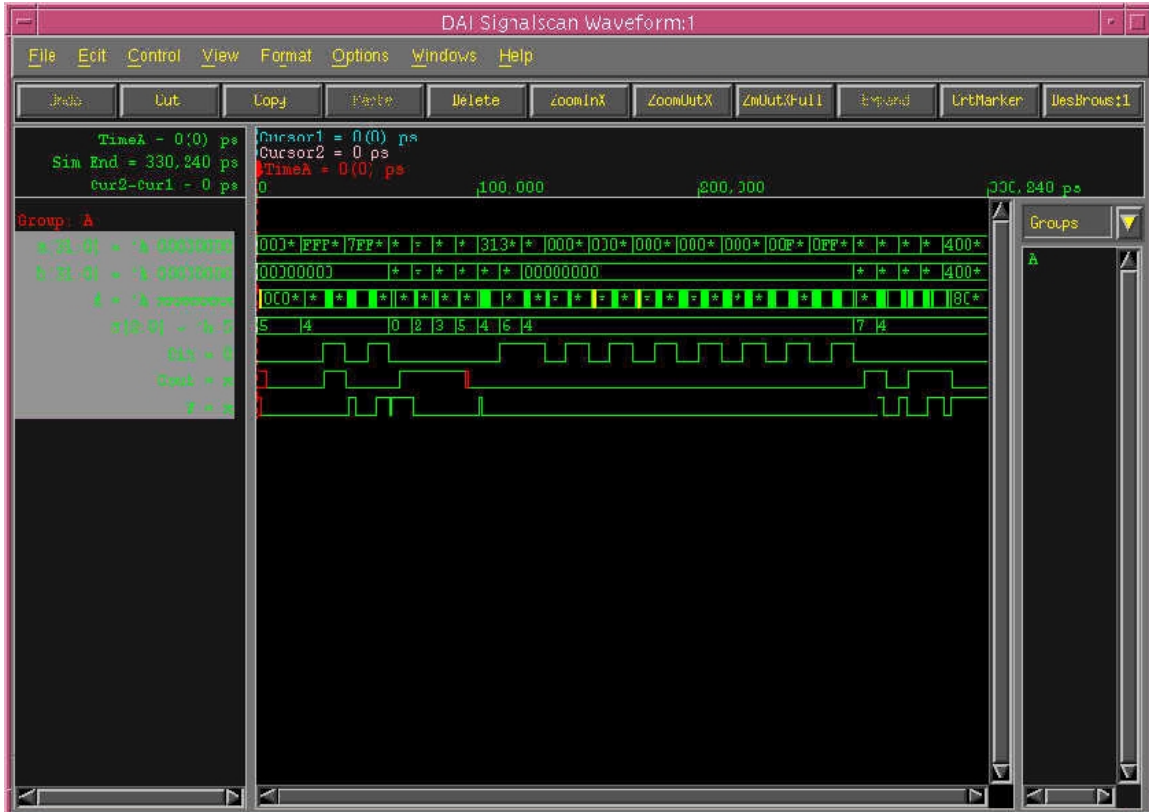
5. In the Signalscan window go to **File-> Open Simulation File...** Select *name.trn* file from the *name.shm* folder.

Example: select the alu32.trn file from the alu32.shm folder.

6. In the Signalscan window, open the Design browser (DesBrows, top right) and select the *name\_testbench* from the **Instances in Current Context** box.

Example: select alu32\_testbench

7. Left click all the ports that are to be viewed from the **Nodes/Variables in Current Context** box in the Design Browser window. Click **Add,Close** button (top right). The Signalscan window shows the waveforms for the inputs, outputs and the nodes similar to the one shown below.





- C) Repeat the steps for **signalscan&** to get an output similar to the one shown below.  
 (Note: Remove or comment the new pins from internal nodes before submitting to the automatic grader.)

