

ECEN 5253

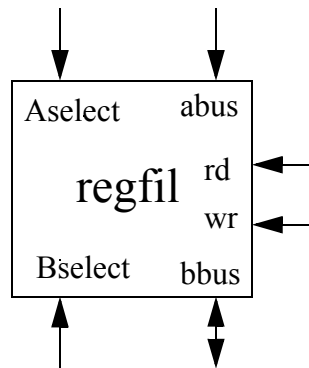
Fall 2006

Design Project 3

Add a register file to your design from project 2. Your design should run at a 100 MHz clock rate (a full clock cycle is 10 nsec. and a half cycle is 5 nsec.).

Part a: Due Fri., Oct. 13, 1700 hrs.

The register file should be designed with latches as discussed in the class notes and have the following inputs and outputs.



The bbus is bidirectional and should be declared as follows.

```
inout [31:0] bbus;
```

The timing requirements of the latches makes the register file model more consistent with a realistic register file based on a static RAM design. The operation of the bi-directional bbus on the register file is controlled by the rd and wr control lines as follows.

| rd | wr | function |
|----|----|--|
| 0 | 0 | bbus not used by register file |
| 0 | 1 | write bbus into register selected by Bselect |
| 1 | 0 | read register selected by Bselect onto bbus |
| 1 | 1 | not allowed |

You must submit a list of all Verilog files in a file named regfil.ver and your high level Verilog file must be named regfil.v. Other Verilog files can be named as you wish. When using the autograder, be sure to use the correct class and assignment name (spelling and case is important!).

class: ecen5253
assignment: proj3a

Part b: Due Fri., Oct. 20, 1700 hrs.

The register file should be connected as shown in Figure 1 to the clocked ALU from

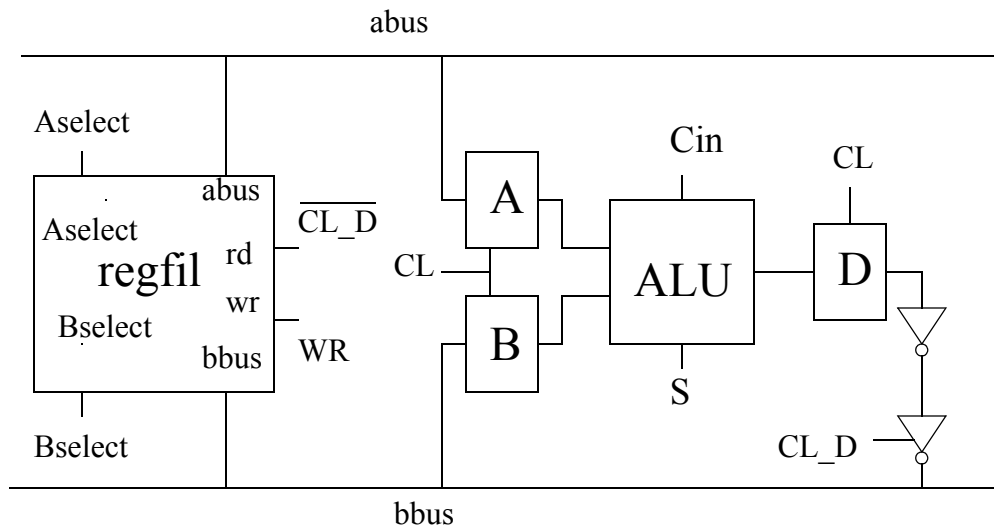


FIGURE 1. Block Diagram

project 2 (the A and B registers are not latches because we are doing a pipelined design). The abus is driven by the register file with the contents of the register selected by the Aselect inputs. When CL is 0, the bbus is driven by the register file with the contents of the register selected by the Bselect inputs. When CL is 1, the register file reads data off the bbus bus and writes it in the register selected by the Bselect inputs. This use of the clock to control reads and writes is the opposite of the unpipelined design, but it will be what we want for the pipelined design.

The wr control line requires special timing because the Bselect lines will change on both rising and falling clock edges as we switch between reading and writing and back again which means

- the wr line cannot go high until after the Bselect lines are correct in order to avoid writing into an incorrect register,
- the wr line must go low before the Bselect lines and the bbus change.

This is a more severe requirement than a level sensitive latch which would not have requirement a. This is a problem for any multi-word memory design. The desired timing for the wr line relative to the clock is shown in Figure 2, and a possible circuit which does it is shown in Figure 3.

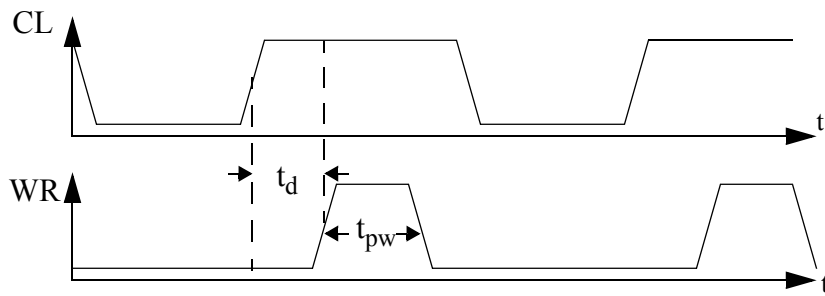


FIGURE 2. WR timing

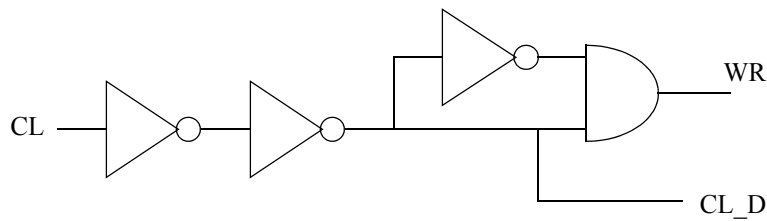


FIGURE 3. Circuit for WR

If t_d is too short, the select lines will not be correct, and you should increase t_d by adding an even number of inverters in series to the first two inverters in Fig. 3. If t_{pw} is too short, the latches in the registers will not operate correctly, and you will need to increase t_{pw} by adding an even number of inverters in series with the top inverter.

Your CPU design should have the terminals shown in Figure 4

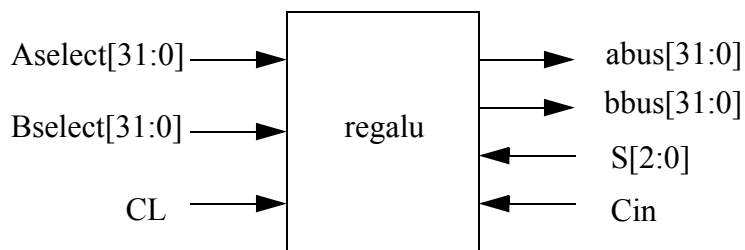


FIGURE 4. CPU Terminals

It will be better to use different internal names for the a-bus and b-bus. The Verilog compiler will complain if you directly connect bbus (an output terminal) to the inputs of the B-register.

The timing on the bbus relative to the clock is shown in Figure 5. It is acceptable for all

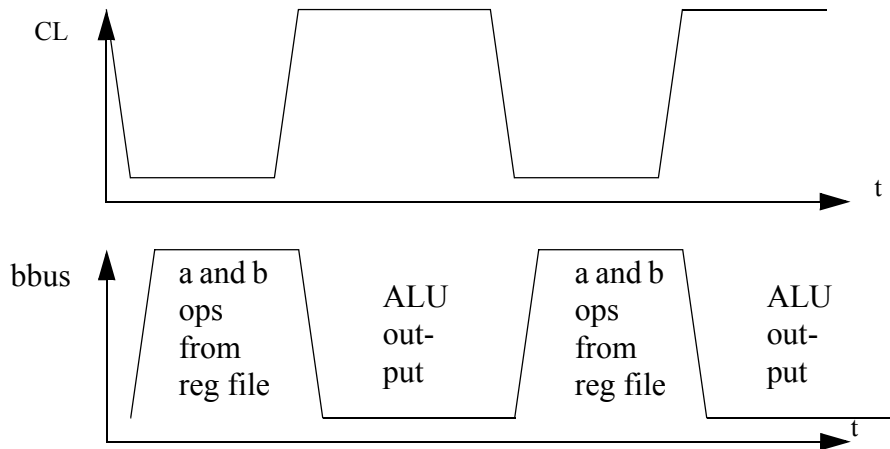


FIGURE 5. Bus Timing

of the latches and registers to remain undefined until something is clocked into them. Note that the timing on the busses requires the bus values to be stable at the clock edges so that the pipeline registers A, B, and D will work correctly. This means that the turn on of the tri-state buffer gates must be delayed relative to CL by using CL_D as in fig. 1.

You must turn in to the automatic grader a list of all Verilog files in a file named regalu.ver and your high level Verilog file must be named regalu.v. Other Verilog files can be named as you wish. When using the automatic grader, be sure to use the correct class and assignment name (spelling and case is important!).

class: ecen5253
assignment: proj3b