

ECEN 5253

Fall 2006

Design Project 2

Due Wed., Oct. 4, 1700 hrs.

Implement the two-bus ALU by putting registers and tri-state buffers around your ALU as shown below. Your design should run at a 100 MHz clock rate (a full clock cycle is 10 nsec. and a half cycle is 5 nsec.). Your circuit should be connected as shown in Figure 1.

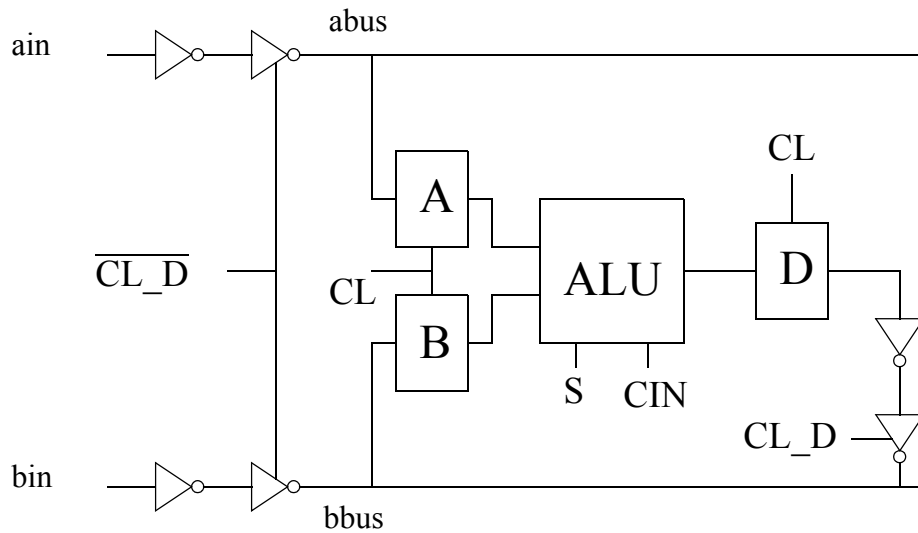


FIGURE 1. Block Diagram

Your CPU design should have the terminals shown in Figure 2

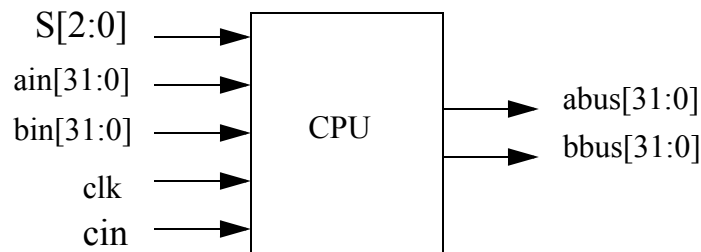


FIGURE 2. CPU Terminals

It will be better to use different internal names for the a-bus and b-bus. The Verilog compiler may complain if you directly connect bbus (an output terminal) to the inputs of the B-register.

The ALU has already been designed in project 1 to provide outputs in less than 10 nsec. The timing on the bbus relative to the clock is shown in Figure 3. It is acceptable for all

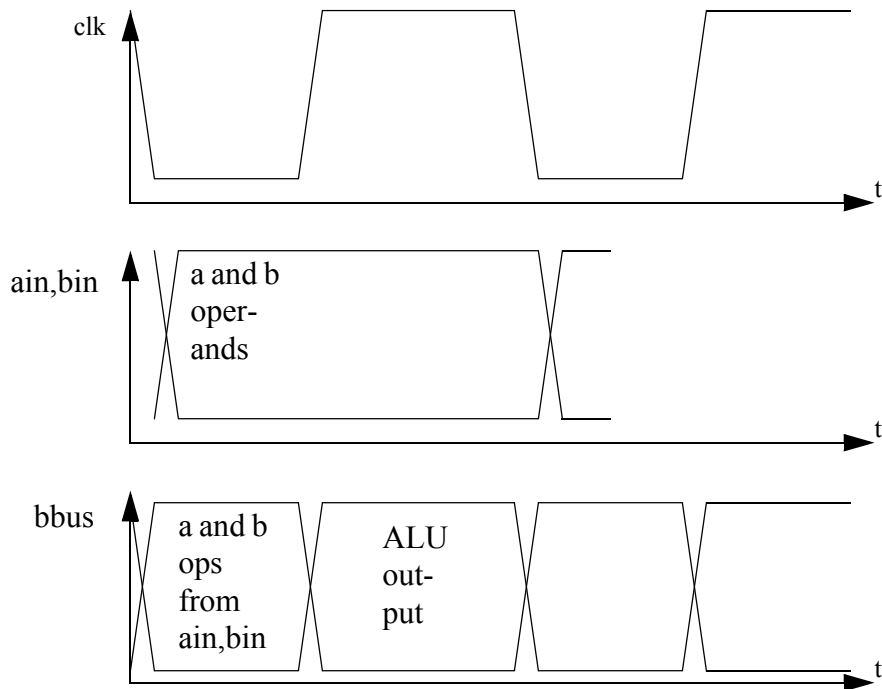


FIGURE 3. Bus Timing

of the registers to remain undefined until something is clocked into them. Note that the timing on the busses requires the bus values to be stable at the rising edge of the clock so that the registers will work correctly. This means that the turn on of the tri-state buffer gates must be delayed relative to CL. A possible circuit which does it is shown in figure 4 (you may need to add more delay). You must use structural Verilog. Do not try synthe-

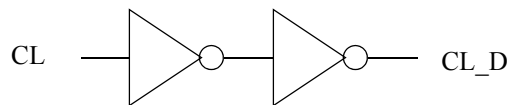


FIGURE 4. Circuit for R/W

size the inverter chain because the synthesizer will optimize the inverters away.

A test bench to provide inputs to your design in

`/x/lgjohn/public/ecen5253/clalu.test.v`

is provided for your convenience in testing your design. A similar file will be used to grade your design.

You must use the web interface to the automatic grader to submit your design for grading. Be sure that all of your structural Verilog files are sent and that a file called clalu.ver is included that lists the names of all of your Verilog files. The highest level Verilog file should be named clalu.v. The clalu.ver is vital since the automatic grading program will NOT grade your design unless it finds this file.

Use the following with the automatic grader (spelling and case is important!).

- project name: proj2
- class name: ecen5253