

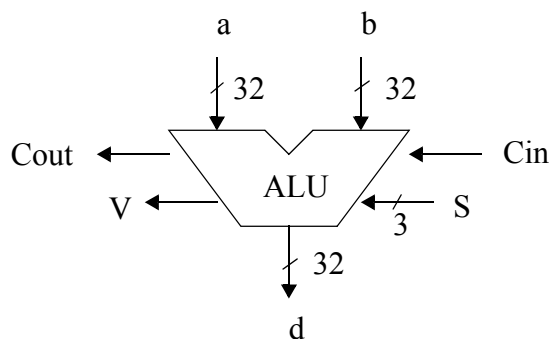
# ECEN 5253

## Fall 2006

### Design Project 1

**Due Mon. Sep. 12, 1700 hrs.**

Use the Cadence VHDL synthesizer to design a 32-bit ALU with a worst case delay of 8 nsec (set the clock frequency in the synthesis file to 100 MHz. The ALU should have the following inputs and outputs.



All busses shall be numbered with 0 as the least significant bit. The inputs and outputs are defined as follows.

- a,b are 32 bit input busses
- d is the 32 bit output buss
- Cin is the carry into bit 0
- Cout is the carry out of bit 31
- V is the overflow output
- S is the 3 bit function select input

The d, Cout and V outputs should implement the correct function according to the following code for the S input.

S	ALU function
000	a xor b
001	a xnor b
010	a + b
011	a - b
100	a or b
101	a nor b
110	a and b
111	X

The ALU function X means that we “don’t care” what the ALU output is for these values of S. You will erroneously generate latches in your ALU if you leave the outputs undefined for these S inputs. Set the outputs to something, e.g. ‘0’; never leave them undefined.

A testbench to provide inputs to your design in

```
/x/lgjohn/public/ecen5253/alu32.test.v
```

is provided for your convenience in testing your design. A similar file will be used to grade your design.

You must use the web interface to the automatic grader to submit your design for grading. Be sure that all of your structural Verilog files are sent and that a file called alu32.ver is included that lists the names of all of your Verilog files. The highest level Verilog file should be named alu32.v. The alu32.ver is vital since the automatic grading program will NOT grade your design unless it finds this file.

Use the following with the automatic grader.

- project name: proj1
- class name: ecen5253